Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A camouflaged circuit structure having a gate region, including: a substrate; a first active region of a first conductivity type being disposed in said substrate; a second active region of a first conductivity type being disposed in said substrate; and a first well of said first conductivity type being disposed in said substrate under said gate region, said first well being in physical contact with said first active region and said second active region, wherein said first well provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit.

2. (currently amended) The camouflaged circuit structure of claim 1 further comprising a plurality of wells of a second type, at least one of said plurality of wells of a second conductivity type being in physical contact with said first active region.

3. (currently amended) The camouflaged circuit structure of claim 2 wherein at least one of said plurality of wells is separated from said first well ~~by a minimum first conductivity type to second conductivity type separation~~.

4. (currently amended) The camouflaged circuit structure of claim 2 wherein said first well is deeper than said plurality of wells of a second conductivity type.

5. (original) The camouflaged circuit structure of claim 1 where said first well is deeper than said first and second active regions.

6. (currently amended) A semiconductor circuit comprising: a substrate having a first well of a first conductivity type; a gate region being arranged above the first well; a

plurality of active regions of said ~~a~~ first conductivity type disposed in said substrate, at least two of said plurality of active regions being separated from one another by, and in physical contact with, said ~~gate region; a~~ first well of said first conductivity type disposed in said substrate under said gate region ~~and in physical contact with said at least two of said plurality of said active regions~~; and a plurality of wells of a second conductivity type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second conductivity type are separated from said first well.